CLAIMS

1. An apparatus comprising:

a first plurality of parallel switches configured to control a voltage on a first output pin; and

a second plurality of parallel switches configured to control a voltage on a second output pin, wherein said first and second pluralities of parallel switches are configured to provide rise time control of a differential waveform and are driven by a phased data signal.

2. The apparatus according to claim 1, wherein a timing between a first and a last phase of said phased data signal is configured to determine a rise and fall time of said differential waveform.

3. The apparatus according to claim 1, wherein each of said first and second pluralities of parallel switches are weighted to determine a pulse shape of said differential waveform.

4. The apparatus according to claim 1, further comprising:

one or more current sources configured to provide current to each of said first and second pluralities of parallel switches.

5. The apparatus according to claim 4, wherein said one or more current sources comprises parallel current sources.

6. The apparatus according to claim 5, wherein each of said parallel current sources are weighted to determine a pulse shape of said differential waveform.

7. The apparatus according to claim 1, further comprising:

a first driver configured in parallel; and

a second driver configured in parallel, wherein said first and second drivers are configured to synchronize to a phased clock signal.

8. The apparatus according to claim 7, wherein said first and second drivers are configured to perform pre-emphasis on said differential waveform.

9. The apparatus according to claim 8, wherein said first and second drivers are configured to mitigate effects of ISI.

10. The apparatus according to claim 7, wherein said first driver comprises a main driver and said second driver comprises a secondary driver.

11. The apparatus according to claim 7, wherein said first driver comprises one or more flip-flops and said second driver comprises one or more flip-flops.

12. The apparatus according to claim 7, wherein said first and second drivers are clocked by a multiphase clock signal.

13. The apparatus according to claim 12, further comprising:

a clock generation circuit configured to generate said multiphase clock in response to a data signal and a precompensation signal.

14. The apparatus according to claim 13, wherein said clock generation circuit is configured to generate said multiphase clock in response to a data transaction on said data signal.

15. The apparatus according to claim 13, wherein a first phase and a second phase of said multiphase clock signal are configured to set a rise and fall time for said differential waveform.

16. The apparatus according to claim 13, wherein generation of said first phase and said second phase are controlled by a bias.

17. The apparatus according to claim 1, wherein said apparatus is configured to overcome cable induced effects.

18. The apparatus according to claim 1, wherein said apparatus is further configured to synchronize a plurality of drivers to provide precompensation.

19. An apparatus comprising:

means for controlling a voltage on a first output pin with a first plurality of parallel switches;

means for controlling a voltage on a second output pin with a second plurality of parallel switches; and

means for providing rise time control of a differential waveform, wherein said first and second pluralities of parallel switches are driven by a phased data signal.

20. A method for SCSI equalization, comprising the steps of:

(A) controlling a voltage on a first output pin with a first plurality of parallel switches;

(B) controlling a voltage on a second output pin with a second plurality of parallel switches; and

(C) providing rise time control of a differential waveform, wherein said first and second pluralities of parallel switches are driven by a phased data signal.